

WHAT IS CLAIMED IS:

1 1. A data routing unit comprising:
2 a data receiver;
3 a data transmitter; and
4 a bridge circuit connected to supply data to said data
5 receiver and to receive data from said data transmitter, said
6 bridge circuit connected to at least one set of data input
7 lines and at least one set of data output lines, said bridge
8 circuit responsive to a header of a data packet received from
9 said data transmitter or received from said at least one set
10 of data input lines to selectively route said received data
11 packet to (1) said data receiver circuit, (2) a selected set
12 of said at least one data output lines, or (3) both said data
13 receiver circuit and a selected set of said at least one set
14 of data output lines dependent upon said header.

1 2. The data routing unit of claim 1, further comprising:
2 an input/output memory connected to said data receiver
3 for storing data received by said data receiver and to said
4 data transmitter for storing data to be transmitted by said
5 data transmitter.

1 3. The data routing unit of claim 2, further comprising:
2 a central processing unit connected said input/output
3 memory for storing data into said input/output memory and
4 reading data from said input/output memory.

1 4. The data routing unit of claim 1, wherein:
2 said at least one set of data input lines consists of a
3 right set of data input lines and a left set of data input
4 lines; and
5 said at least one set of data output lines consists of a
6 right set of data output lines and a left set of data input
7 lines.

1 5. The data routing unit of claim 1, wherein:
2 each of said at least one set of data output lines
3 consists of a plurality of data lines and a data routing unit
4 clock line; and
5 said data transmitter generating data transmitted on said
6 data lines synchronous with a transmitter clock signal on said
7 data routing unit clock line.

1 6. The data routing unit of claim 5, further comprising:
2 an input/output memory connected to said data receiver
3 for storing data received by said data receiver and to said
4 data transmitter for storing data to be transmitted by said
5 data transmitter; and
6 a central processing unit connected said input/output
7 memory for storing data into said input/output memory and
8 reading data from said input/output memory, said central
9 processing unit operating in synchronism with a CPU clock
10 which is asynchronous with said transmitter clock signal.

1 7. The data routing unit of claim 1, wherein:
2 each of said at least one set of data input lines
3 consists of a plurality of data lines and a data routing unit
4 clock line; and
5 said data receiver sensing data received on said data
6 lines synchronous with a transmitter clock signal on said data
7 routing unit clock line.

1 8. The data routing unit of claim 7, further comprising:
2 an input/output memory connected to said data receiver
3 for storing data received by said data receiver and to said
4 data transmitter for storing data to be transmitted by said
5 data transmitter; and
6 a central processing unit connected said input/output
7 memory for storing data into said input/output memory and
8 reading data from said input/output memory, said central
9 processing unit operating in synchronism with a CPU clock
10 which is asynchronous with said transmitter clock signal.

1 9. The data routing unit of claim 1, wherein:
2 said bridge circuit further includes
3 a node address register storing a uniquely assigned
4 multibit node address;
5 a node address comparator connected to said node
6 address register for comparing predetermined destination
7 node address bits of said header with said node address
8 stored in said node address register; and
9 said bridge circuit selectively routing said
10 received data packet to said data receiver when said
11 destination node address bits matches said node address.

1 10. The data routing unit of claim 9, wherein:
2 said bridge circuit further includes
3 a plurality of routing registers, each routing
4 register corresponding to one set of data output lines,
5 each routing register storing an indication of a set of
6 node addresses;
7 a plurality of routing comparators, each routing
8 comparator connected to a corresponding routing register
9 for comparing predetermined destination node address bits
10 of said header with said indication of as set of node
11 addresses stored in said corresponding routing register;
12 and
13 said bridge circuit selectively routing said
14 received data packet to a set of data output lines when
15 said destination node address bits matches a node address
16 of said set of node addresses stored in said
17 corresponding routing register.

1 11. The data routing unit of claim 9, wherein:
2 said at least one set of data input lines consists of a
3 right set of data input lines and a left set of data input
4 lines;
5 said at least one set of data output lines consists of a
6 right set of data output lines and a left set of data input
7 lines;
8 said bridge circuit further includes
9 a right routing register storing a right routing
10 data word having a plurality of bits, each bit
11 corresponding to a unique node address and having either

12 a first digital state indicating routing via said right
13 data output lines to reach said unique node address or a
14 second digital state indicating not routing via said
15 right data output lines to reach said unique node
16 address;

17 a left routing register storing a left routing data
18 word having a plurality of bits, each bit corresponding
19 to a unique node address and having either a first
20 digital state indicating routing via said left data
21 output lines to reach said unique node address or a
22 second digital state indicating not routing via said left
23 data output lines to reach said unique node address;

24 a decoder receiving said header for converting said
25 destination node address into a multibit destination data
26 word having a bit corresponding to said destination node
27 address in said first digital state and all other bits in
28 said second digital state;

29 a right comparator connected to said right routing
30 register and said decoder for comparing said right
31 routing data word and said destination data word; and

32 a left comparator connected to said left routing
33 register and said decoder for comparing said left routing
34 data word and said destination data word; and

35 said bridge circuit selectively routing said
36 received data packet to said right data output lines when
37 said destination data word matches said right routing
38 data word and selectively routing said received data
39 packet to said left data output lines when said
40 destination data word matches said left routing data
41 word.

1 12. The data routing unit of claim 11, further
2 comprising:

3 an input/output memory connected to said data receiver
4 for storing data received by said data receiver and to said
5 data transmitter for storing data to be transmitted by said
6 data transmitter; and

7 a central processing unit connected said input/output
8 memory for storing data into said input/output memory and
9 reading data from said input/output memory, said central
10 processing unit operable to write data into said right routing
11 register and into said left routing register.

1 13. The data routing unit of claim 1, wherein:

2 said at least one set of data input lines consists of a
3 right set of data input lines and a left set of data input
4 lines;

5 said at least one set of data output lines consists of a
6 right set of data output lines and a left set of data input
7 lines;

8 said bridge circuit selectively routing said received
9 data packet to said data receiver when a predetermined central
10 navigation bit of said header has a first digital state,
11 routing said received data packet with said header deleted to
12 said right set of data output line when a predetermined right
13 navigation bit of said header has said first digital state and
14 routing said received data packet with said header deleted to
15 said left set of data output line when a predetermined left
16 navigation bit of said header has said first digital state.